Amendments to the Claims:

1-24. (Canceled)

25. (Previously Amended) An enhanced VSB receiver for receiving and decoding a terrestrial broadcasting signal transmitted from a VSB transmitter, the enhanced VSB receiver comprising:

a VSB demodulator for receiving an input signal including main data and enhanced data from the VSB transmitter and converting the input signal into a base band signal;

a data attribute generator for generating data attribute information indicating whether each symbol included in the input signal corresponds to the main or enhanced data;

a trellis decoder for providing at least one of a slicer prediction signal and a prediction reliability signal by using the data attribute information; and

a phase tracker for correcting a phase of the base band signal by using the data attribute information and the slicer prediction signal.

26. (Previously Amended) The enhanced VSB receiver of claim 25, further comprising a channel equalizer which corrects a distorted channel in the base band signal by using the slicer prediction signal, the prediction reliability signal, and the data attribute information.

27. (Previously Amended) The enhanced VSB receiver of claim 25, wherein the trellis decoder decodes the phase-corrected signal outputted from the phase tracker by using a Viterbi decoding algorithm and the data attribute information.

28. (Previously Added) The enhanced VSB receiver of claim 27, further comprising:

a data deinterleaver for deinterleaving the Viterbi-decoded signal outputted from the trellis decoder;

a Reed-Solomon decoder for decoding the deindeterleaved signal outputted from the data deinterleaver; and

a data derandomizer for derandomizing the Reed-Solomon-decoded signal outputted from the Reed-Solomon decoder.

29. (Previously Added) The enhanced VSB receiver of claim 28, wherein the Reed-Solomon decoder removes 20 parity bytes from the deinterleaved signal outputted from the data deinterleaver without subjecting the enhanced data to Reed-Solomon decoding.

30. (Previously Added) The enhanced VSB receiver of claim 25, further comprising a comb filter for removing an NTSC interference signal from the base band signal converted by the demodulator.

31. (Previously Amended) The enhanced VSB receiver of claim 25, further comprising a main data remover for removing the main data from the phase-corrected signal outputted from the phase tracker to output the enhanced data.

32. (Previously Added) The enhanced VSB receiver of claim 25, wherein the demodulator recovers a segment synchronizing signal, a field synchronizing signal, and a symbol timing from the base band signal.

33. (Previously Amended) The enhanced VSB receiver of claim 32, further comprising a main data remover for removing the main data from the phase-corrected signal to output the enhanced data according to multiplexing information detected from the field synchronizing signal recovered by the demodulator.

34. (Previously Added) The enhanced VSB receiver of claim 25, further comprising:

a demultiplexer for demultiplexing the phase-corrected signal outputted from the phase tracker into the main data and the enhanced data; and

a supplemental VSB processor for decoding the enhanced data demultiplexed from the demultiplexer to obtain original data.

35. (Currently Amended) The enhanced VSB receiver of claim 34, wherein the supplemental VSB processor comprises:

a header remover for removing header bytes from the enhanced data received from the demultiplexer;

a null data remover for removing a plurality of null bits from the header-removed data; and

a Reed-Solomon decoder for subjecting ~~the~~ null-bit-removed ~~null-data-removed~~ data to Reed-Solomon decoding.

36. (Previously Amended) The enhanced VSB receiver of claim 26, wherein the channel equalizer comprises:

a plurality of slicers, each slicer having a predetermined signal level detector;

a feed-forward filter for receiving the base band signal from the demodulator;

a feedback filter for receiving an output signal of one of the plurality of slicers;

an adder for adding output signals of the feed-forward filter and the feedback filter and outputting an added signal as a channel equalizer output signal, wherein the plurality of slicers commonly receive the added signal;

a multiplexer for outputting one of the outputs of the plurality of slicers to the feedback filter in response to a control signal; and

a controller for updating filter coefficients of the feed-forward filter and the feedback filter and providing the control signal to the multiplexer in response to a multiplexer output signal, the slicer prediction signal, and the prediction reliability signal, and the channel equalizer output signal to select the multiplexer to output signal from one of the plurality of slicers that has the predetermined signal level detector closes to the based band signal.

37. (Currently Amended) The enhanced VSB receiver of claim 36, further ~~comprises~~ comprising a slicer predictor which receives the channel-corrected signal and the data attribute information, estimates a register value of ~~the~~ a trellis coder, calculates prediction reliability, and forwards the estimated register value to the controller of the channel equalizer.

38. (Previously Added) The enhanced VSB receiver of claim 37, wherein the plurality of slicers includes first to third slicers for processing main data symbols, and forth to nine slicers for processing the enhanced data symbols, wherein the first slicer has 8 level values of -7, -5, -3, -1, +1, +3, +5, +7, the second slicer has 4 level values of -7, -3, +1, +5, the third slicer has 4 level values of -5, -1, +3, +7, the fourth slicer has 4 level values of -7, -5, +1, +3, the fifth slicer has 4 level values of -3, -1, +5, +7, the sixth slicer has 2 level values of -7, +1, the seventh slicer has 2 level values of -5, +3, the eighth slicer has 2 level values of -3, +5, and the ninth slicer has 2 level values of -1, +7.

39. (Currently Amended) The enhanced VSB receiver of claim 38, wherein with respect to the main data symbols, the first slicer is selected in a low reliability case, the second slicer is selected for a high reliability case and the estimated register value is at a first logic level, and the third slicer is selected for a high reliability case and the estimated register value is at a second logic level.

40. (Previously Added) The enhanced VSB receiver of claim 38, wherein with respect to the enhanced data symbols;

one of the fourth slicer and the fifth slicer is selected in response to the null bit value for a low reliability case;

the sixth slicer is selected for a high reliability case and the null bit value and the estimated register value are at a first logic level;

the seventh slicer is selected for a high reliability case and the null bit value is at a first logic level and the estimated register value is at a second logic level;

the eighth slicer is selected for a high reliability case and the null bit value is a second logic level and the estimated register value is at a first logic level; and

the ninth slicer is selected for a high reliability case and the null bit value and the estimated register value are at a second logic level.

41. (Previously Added) The enhanced VSB receiver of claim 25, wherein the main data included in the input signal comprises MPEG data.

42. (Previously Amended) The enhanced VSB receiver of claim 25, wherein the data attribute generator comprises:

a multiplexer for receiving and multiplexing an enhanced data dummy packet and a main data dummy packet and outputting as a multiplexer output signal;

a randomizer for randomizing the multiplexer output signal;

a parity inserter for inserting dummy bytes to the randomized data;

a data interleaver for interleaving an output of the parity inserter; and

a trellis coder for converting the interleaved data to symbols and outputting the converted symbols without subjecting to trellis coding.

43. (Previously Added) The enhanced VSB receiver of claim 42, wherein each symbol outputted from the trellis coder includes a bit D1, wherein if the bit D1 is at a first logic level, a corresponding symbol included in the input signal corresponds to a enhanced data symbol, and if the bit D1 is at a second logic level, the symbol corresponds to a main data symbol.

44. (Previously Amended) The enhanced VSB receiver of claim 42, wherein each symbol outputted from the trellis coder includes two bits D1 and D0, wherein if the bit D1 is at a first logic level, the bit D0 represents a corresponding one of a plurality of null bits included in the enhanced data.

45. (Previously Amended) A method of receiving and decoding a terrestrial broadcasting signal for a VSB receiver, the method comprising:

receiving an input signal including main data and enhanced data from a VSB transmitter and converting the received input signal into a base band signal;

generating data attribute information indicating whether each symbol included in the input signal corresponds to the main data or enhanced data;

providing at least one of a slicer prediction signal and a prediction reliability signal by using the data attribute information; and

correcting a phase of the base band signal using data attribute information and the slicer prediction signal.

46. (Previously Amended) The method of claim 45, further comprising correcting a distorted channel in the base band signal by using the slicer prediction signal, the prediction reliability signal, and the data attribute information.

47. (Previously Amended) The method of claim 45, further comprising decoding the phase-corrected signal by using a Viterbi decoding algorithm and the data attribute information.

48. (Previously Amended) The method of claim ~~23~~ 47, further comprising:

deinterleaving the Viterbi-decoded signal;

Reed-Solomon decoding the deinterleaved signal; and

derandomizing the Reed-Solomon-decoded signal.

49. (Previously Added) The method of claim 45, further comprising removing an NTSC interference signal from the base band signal if the NTSC interference signal is detected.

50. (Previously Added) The method of claim 45, further comprising:

demultiplexing the phase-corrected signal into the main data and the enhanced data; and

decoding the demultiplexed enhanced data to obtain original data.

51. (Previously Amended) The method of claim 50, wherein the converting the received input signal into a base band signal comprises recovering at least one of a segment synchronizing signal, a field synchronizing signal, and a symbol timing from the base band signal.

52. (Previously Added) The method of claim 51, wherein the demultiplexing the phase-corrected signal into the main data and the enhanced data comprises:

detecting multiplexing information included in the recovered field synchronizing signal; and

demultiplexing the phase-corrected signal into the main data and the enhanced data according to the detected multiplexing information.

53. (Currently Amended) The method of claim 50, wherein the decoding the demultiplexed enhanced data to obtain original data comprises:

removing header bytes from the demultiplexed enhanced data;

removing a plurality of null bits included in the header-removed data; and

Reed-Solomon decoding ~~the null-data-removed~~null-bit-removed data to obtain the original data.

54. (Previously Amended) The method of claim 45, wherein the generating data attribute information comprises:

receiving and multiplexing an enhanced dummy packet and a main data dummy packet and outputting as a multiplexer output signal;

randomizing the multiplexer output signal;

inserting dummy bytes to the randomized signal;

interleaving the dummy-byte-inserted signal; and

converting the interleaved signal into symbols and outputting the symbols without subjecting the trellis coding.

55. (Previously Added) The method of claim 54, wherein each converted symbol includes a bit D1, wherein if the bit D1 is at a first logic level, a corresponding symbol included

in the input signal corresponds to a enhanced data symbol, and if the bit D1 is at a second logic level, the symbol corresponds to a main data symbol.

56. (Previously Amended) The method of claim 54, wherein each converted symbol includes two bits D1 and D0, wherein if the bit D1 is at a first logic level, the bit D0 represents a corresponding one of a plurality of null bits included in the enhanced data.